

## CLAIMS

What is claimed is:

- 1 1. An integrated circuit fabricated on a chip, comprising:  
2 at least one source device in the integrated circuit generating internal state data at a first  
3 frequency;  
4 an output port that drives data to external logic at a second frequency that is lower than said  
5 first frequency; and  
6 wherein said output port includes a bandwidth manager that selects internal state data that  
7 is most important to drive to said external logic during periods when said output port becomes  
8 saturated, and which selects all internal state data to drive to said external logic during periods  
9 when said output port is not saturated .  
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1 5. The system of claim 2, wherein multiple output ports are provided in said processor, at  
2 least one of which includes a bandwidth manager.

1 6. The system of claim 2, wherein output port includes an output driver that drives internal  
2 state data selected by the bandwidth manager to said external logic.

1 7. The system of claim 6, wherein the bandwidth manager includes selection logic that selects  
2 data from one or more sources to pass to said output driver.

1 8. The system of claim 7, wherein the selection logic comprises a multiplexer.

1 9. The system of claim 7, wherein the selection logic assigns an importance level to each tick  
2 of said internal state data, which is used by said bandwidth manager to determine whether the tick  
should be selected for transmission to external logic when the output port is saturated.

1 10. The system of claim 9, wherein the selection logic adds at least one control bit to each tick  
2 indicating the importance level of that tick.

1 11. The system of claim 9, wherein the selection logic also adds a control bit to each tick  
2 indicating if the tick represents valid data.

1 12. The system of claim 11, wherein the bandwidth manager further includes a smart buffer  
2 coupled to said selection logic, and wherein said selection logic presents a tick to said smart buffer  
3 at said first frequency.

1 13. The system of claim 12, wherein the smart buffer has a plurality of slots for storing ticks,  
2 and wherein said smart buffer periodically unloads a tick at the second clock frequency to pass to  
3 said output driver.

1 14. The system of claim 13, wherein the smart buffer is configured as a first-in, first-out  
2 memory buffer, and wherein said smart buffer accepts the tick presented by said selection logic if a  
3 first slot in said smart buffer is empty.

1 15. The system of claim 14, wherein the smart buffer accepts the tick presented by said  
2 selection logic if the smart buffer is concurrently unloading a tick to pass to said output driver.

1 16. The system of claim 14, wherein the smart buffer accepts the tick presented by said  
2 selection logic if the importance level of the presented tick is greater than the importance level of  
3 the tick stored in the first slot of said memory buffer, and wherein said smart buffer overwrites the  
4 value of the presented tick in said first slot.

1 17. The system of claim 14, wherein the smart buffer determines if any slots are empty, and if  
2 so, advances ticks stored in full slots to fill the empty slots.

1 18. The system of claim 17, wherein the full ticks are advanced on at a rate equal to said first  
2 frequency.

1 19. The system of claim 14, wherein a plurality of smart buffers are included in said bandwidth  
2 manager which are connected in parallel to process data concurrently.

1 20. The system of claim 19, wherein the selection logic is capable of presenting a tick to each  
2 of said plurality of said smart buffers at a rate equal to said first frequency.

1 21. The system of claim 20, wherein the bandwidth manager further includes arbitration logic  
2 coupled to a last slot of each of said plurality of smart buffers, and wherein said arbitration logic  
3 selects the tick stored in the last slot of one of said smart buffers to unload at said second clock  
4 frequency.

1 22. The system of claim 20, wherein the arbitration logic receives a signal indicating the  
2 importance of the tick in the last slot of each smart buffer, whether the last slot of each smart buffer  
3 is full, and whether each smart buffer is under pressure.

1 23. The system of claim 22, wherein the arbitration logic selects the last tick from a smart  
2 buffer if it is under pressure and the other smart buffer(s) is not.

1 24. The system of claim 22, wherein the arbitration logic selects the last tick which has the  
2 highest importance level.

1 25. The system of claim 21, wherein the arbitration logic selects the last tick from said plurality  
2 of said smart buffers on a round-robin basis.

1 26. The system of claim 1, wherein the first frequency is the frequency of the selected source.

1 27. The system of claim 26, further comprising a clock circuit that automatically determines  
2 the second frequency based on the ratio of the first frequency to an internal system clock.

1 28. The system of claim 27, wherein the clock circuit rounds up the ratio to an integer value to  
2 reduce the second frequency.

1 29. The system of claim 1, wherein the bandwidth manager includes packet prediction logic  
2 which predicts the start of a packet of internal state data, and which assigns an importance value to  
3 each tick of said packet based on the location of the tick in the packet.

1 30. The system of claim 29, wherein the packet prediction logic includes a decoder that  
2 decodes opcodes in a first tick of a packet to identify the length of each packet.

1 31. The system of claim 29, wherein the packet prediction logic synchronizes when a packet  
2 pattern is detected from said source device.

1 32. A processor, comprising:  
2 a plurality of internal source devices generating internal state data at a first frequency;  
3 an output driver that drives data to external logic at a second frequency; and  
4 a bandwidth manager that selects internal state data that is most important to drive to said  
5 external logic during periods when said output port becomes saturated, and which selects all  
6 internal state data to drive to said external logic during periods when said output driver is not  
7 saturated.

1 33. The processor of claim 32, wherein the internal state data sources are organized by regions  
2 within the processor, and internal state data from one or more of the regions are selected by a user  
3 programmable enable signal.

1 34. The processor of claim 32, wherein multiple sets of output drivers and bandwidth managers  
2 are provided in said processor.

1 35. The processor of claim 32, wherein the bandwidth manager includes selection logic that  
2 selects data from one or more sources to pass to said output driver.

1 36. The processor of claim 35, wherein the selection logic assigns an importance level to each  
2 tick of said internal state data, which is used by said bandwidth manager to determine whether the  
3 tick should be selected for transmission to external logic when the output driver is saturated.

1 37. The processor of claim 36, wherein the selection logic adds at least one control bit to each  
2 tick indicating the importance level of that tick.

1 38. The processor of claim 37, wherein the selection logic also adds a control bit to each tick  
2 indicating if the tick represents valid data.

1 39. The processor of claim 38, wherein the bandwidth manager further includes a smart buffer  
2 coupled to said selection logic, and wherein said selection logic presents a tick to said smart buffer  
3 at said first frequency.

1 40. The processor of claim 12, wherein the smart buffer has a plurality of slots for storing ticks,  
2 and wherein said smart buffer periodically unloads a tick at the second clock frequency to pass to  
3 said output driver.

1 41. The processor of claim 40, wherein the smart buffer is configured as a first-in, first-out  
2 memory buffer, and wherein said smart buffer accepts the tick presented by said selection logic if a  
3 first slot in said smart buffer is empty.

1 42. The processor of claim 41, wherein the smart buffer accepts the tick presented by said  
2 selection logic if the smart buffer is concurrently unloading a tick to pass to said output driver.

1 43. The processor of claim 41, wherein the smart buffer accepts the tick presented by said  
2 selection logic if the importance level of the presented tick is greater than the importance level of  
3 the tick stored in the first slot of said memory buffer, and wherein said smart buffer overwrites the  
4 value of the presented tick in said first slot.

1 44. The processor of claim 41, wherein the smart buffer determines if any slots are empty, and  
2 if so, advances ticks stored in full slots to fill the empty slots.

1 45. The processor of claim 44, wherein the full ticks are advanced on at a rate equal to said first  
2 frequency.

1 46. The processor of claim 41, wherein a plurality of smart buffers are included in said  
2 bandwidth manager which are connected in parallel to process data concurrently.

1 47. The processor of claim 46, wherein the selection logic is capable of presenting a tick to  
2 each of said plurality of said smart buffers at a rate equal to said first frequency.

1 48. The processor of claim 47, wherein the bandwidth manager further includes arbitration  
2 logic coupled to a last slot of each of said plurality of smart buffers, and wherein said arbitration



3 logic selects the tick stored in the last slot of one of said smart buffers to unload at said second  
4 clock frequency.

1 49. The processor of claim 48, wherein the arbitration logic receives a signal indicating the  
2 importance of the tick in the last slot of each smart buffer, whether the last slot of each smart buffer  
3 is full, and whether each smart buffer is under pressure.

1 50. The processor of claim 49, wherein the arbitration logic selects the last tick from a smart  
2 buffer if it is under pressure and the other of said plurality of smart buffers are not.

1 51. The processor of claim 49, wherein the arbitration logic selects the last tick which has the  
2 highest importance level.

1 52. The processor of claim 49, wherein the arbitration logic selects the last tick from said  
2 plurality of said smart buffers on a round-robin basis.

1 53. The processor of claim 32, wherein the first frequency is the frequency of the selected  
2 source.

1 54. The processor of claim 53, further comprising a clock circuit that automatically determines  
2 the second frequency based on the ratio of the first frequency to an internal processor clock.

1 55. The processor of claim 54, wherein the clock circuit rounds up the ratio to an integer value  
2 to reduce the second frequency.

1 56. The processor of claim 43, wherein the selection logic includes packet prediction logic  
2 which predicts the start of a packet of internal state data, and which assigns said importance value  
3 to each tick of said packet based on the location of the tick in the packet.

1 57. The processor of claim 56, wherein the packet prediction logic includes a decoder that  
2 decodes opcodes in a first tick of a packet to identify the length of each packet.

1 58. The processor of claim 57, wherein the packet prediction logic synchronizes when a packet  
2 pattern is detected from said source device.

1 59. An integrated circuit fabricated on a chip, comprising:  
2 at least two source devices in the integrated circuit, each of which is capable of generating  
3 internal state data at a first frequency;  
4 an output port that drives data to external logic at said first frequency; and  
5 wherein said output port includes a bandwidth manager that selects internal state data that  
6 is most important to drive to said external logic during periods when said output port becomes  
7 saturated, and which selects all internal state data to drive to said external logic during periods  
8 when said output port is not saturated .

1 60. An integrated circuit fabricated on a chip, comprising:

2 at least one source device in the integrated circuit generating internal state data at a first  
3 frequency;  
4 an output port that drives data to external logic at a second frequency; and  
5 wherein said output port includes at least one smart buffer that examines each newly  
6 presented tick of internal state data and determines the relative importance of that tick as compared  
7 to the relative importance of the last previously stored tick.

1 61. The system of claim 60, wherein the smart buffer permits more important ticks to advance  
2 through the smart buffer with a tail-eating type of action in instances where the output port  
3 becomes saturated.

4 62. The system of claim 60, wherein the smart buffer permits all valid ticks to advance through  
5 the smart buffer in instances where the output port is not saturated.

6 63. The processor of claim 60, wherein the second frequency is substantially less than said first  
7 frequency.

1 64. The processor of claim 60, wherein the second frequency is substantially the same as the  
2 first frequency.

1 65. The processor of claim 32, wherein the second frequency is substantially less than said first  
2 frequency.

1 66. The processor of claim 32, wherein the second frequency is substantially the same as the  
2 first frequency.

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